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Design of Complex Inter Connection Matrix Using Advanced Bus Architecture

Roopa M, Vani R.M, P.V.Hunagund

Abstract— The Advanced Microcontroller Bus Architecture (AMBA) is widely used interconnection standard for System on chip (SOC). Advanced High performance Bus (AHB) is a new generation of AMBA bus, which is intended to address the requirements of high – performance synthesizable designs.Multilayer AHB is an interconnection scheme,based on the AHB protocol that enables parallel access path between the multiple masters and slaves ina system. This is achieved by using a more complex interconnection matrix and gives the benefit of increased overall bus bandwidth and more flexible system architecture.In This paper we used HDL (Hardware Description Language) for designing the RTL (Register Transfer Level) code.Synthesis and simulation is done using Xilinx and Modelsim.

Index Terms— System-on-chip (SOC), Advanced Microcontroller Bus Architecture (AMBA), Advanced High performance Bus (AHB)

1 INTRODUCTION

System-on-a-Chip (SoC) design refers to implementing an entire electronic sub-system on a single integrated circuit (IC). Smaller feature sizes makes adding extra circuitry on silicon die more cost-effective. Chips manufactured with these dies consist of one (or more) processor(s), a high-performance bus, custom logic (digital and analog), memory devices and peripherals along with software code. SoC design requires developing innovative techniques to tackle design complexity and its related risks[1].

The Advanced Microcontroller Bus Architecture (AMBA) is a widely used interconnection standard or System on Chip (SoC) design [2]. In order to support high-speed pipelined data transfers, AMBA supports a rich set of bus signals, making the analysis of AMBA-based embedded systems a challenging proposition. The AMBA specification has become a de facto standard for the semiconductor industry, and has been adopted by more than 95% of Arm's partners and a number of IP providers. The specification has been successfully implemented in several ASIC designs [2].

Since the AMBA interface is processor and technology independent, it enhances the reusability of peripheral and system components across a wide range of applications. The AMBA specification defines three Buses/Interfaces:

- Advanced High Performance Bus (AHB)
- Advanced System Bus(ASB)
- Advanced Peripheral Bus (APB)

- *Roopa M Associate Professor Department of Electronics and Cummunication Engineerign, DSCE, Bangalore, INDIA,. PH-9449229242. E-mail:surajroopa@gmail.com*
- *Dr Vani R M Professor and HOD University science Intrumentation Center, Gulbarga Univesity, Gulbarga, INDIA .PH-9342331758. E-mail: vanirm12@rediffmail.com*
- Dr P V Hunagund Professor, Department of Applied Electronics, Gulbarga University, Gulbarga, INDIA .PH-9845372523

2 BUS INTERCONECTION

The AMBA AHB bus protocol is designed to be used with a central multiplexer interconnection scheme. Using this scheme all bus masters drive out the address and control signals indicating the transfer they wish to perform and the arbiter determines which master has its address and control signals routed to all of the slaves. A central decoder is also required to control the read data and response signal multiplexer, which selects the appropriate signals from the slave that is involved in the transfer. Figure 1 illustrates the structure required to implement an AMBA AHB design with three masters and four slaves [3].

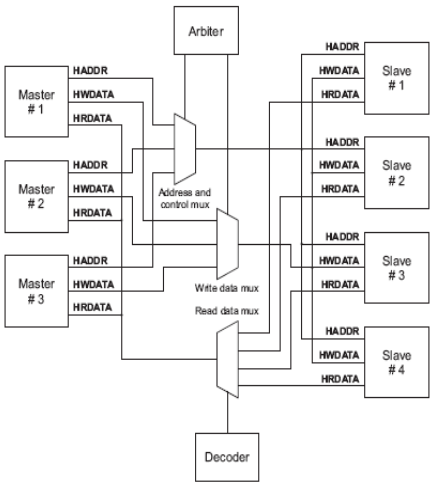

Fig1: Typical AMBA AHB design with 3 Masters and 4 Slaves.

The multi-layer bus architecture has a number of benefits:
It allows development of multi-master systems with an increased available bus bandwidth.

- Complex multi-master systems can be constructed which have a flexible architecture. This removes the requirement

to fix design decisions about the allocation of system resources to particular masters at the hardware design stage.

- Each AHB layer can become very simple because it has only one master ,so no arbitration or master-to-slave muxing is required .These layers can use the AHB-LITE protocol, meaning that they do not have to support request and grant , nor do they have to support retry or split operation.
- The arbitration effectively becomes point arbitration at each peripheral and is only necessary when more than one master wants to access the same slave simultaneously.
- The only hardware that has to be added to the standard AHB transport infrastructure is the multiplexor block to connect the multiple masters to the peripherals.
- Because the multi-layer architecture is based on the existing AHB protocol, previously designed masters and slaves can be used without any modification.

3 MULTILAYER-AHB BUS MATRIX

A multilayer AHB system consists mainly of the following components.

- A multilayer AHB master
- A multilayer AHB slave
- Interconnect matrix

The multilayer AHB master generates the address and data to be written into the slave along with various other control signals required for proper transfer of data. The multilayer AHB slave is basically a memory element capable of capturing the address and data sent by the master and also it should perform reading the data from its memory location whose address will be specified by the master. The interconnect matrix is a component which connects many number of masters and slaves. It also determines whether or not a master should be able to perform data transfer with its requesting slave. Features of Interconnect Matrix are: The complete working of the interconnect matrix must be able to operate solely based on address decoding and should not include any specialized signals. The interconnect matrix must also be a combinational network and hence must be independent of any clock input [4].

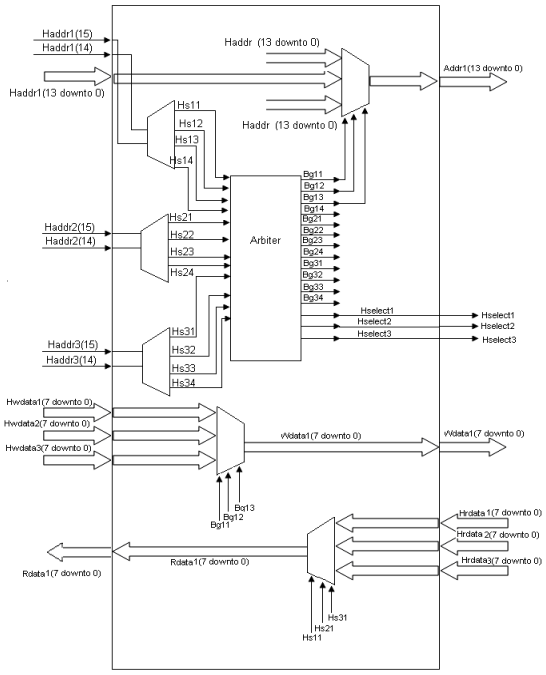

Figure2: Block diagram of Interconnect matrix with internal structure

4 IMPLEMENTATION

Access to the same slave at the same time the arbitration within the interconnect matrix must determine which layer has highest priority. The layer that is not given access is waited until it is allowed access to the required slave. When the layer is waited an input stage is used to store a copy of the pipelined address and control information until access to the shared slave is allowed. Each slave port effectively has its own arbitration and a number of different schemes can be used. Input layers can be serviced in round-robin fashion, changing every transfer or every burst, or the arbitration can use a fixed priority scheme where certain high priority layers are always given access in preference to lower priority layers. The number of input /output ports on the interconnect matrix is completely flexible and can be adapted to suit the system requiremen.

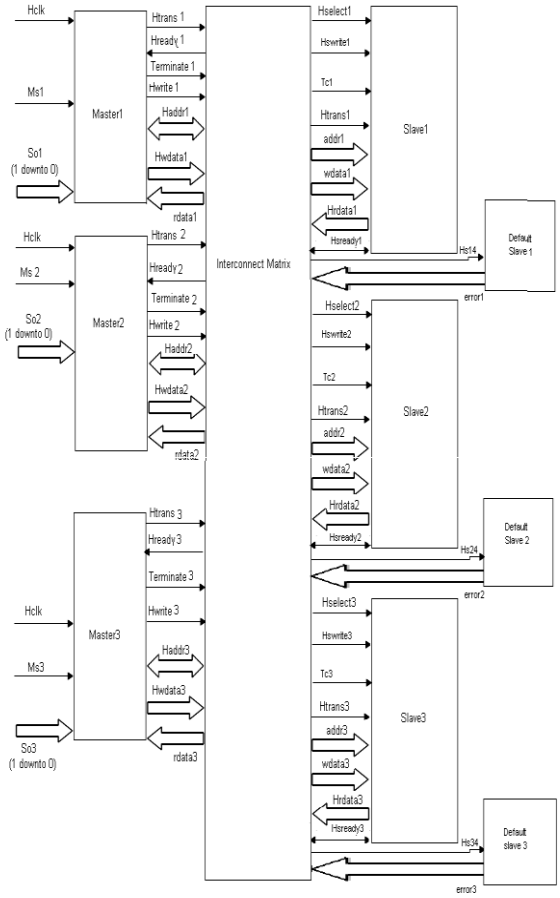

Fig 3: Interconnect matrixes which connect three masters and three slaves.

From the above Figure (3), we can see that it consists of the following components:

1. Three masters
2. Three slaves
3. Three default slaves for each master
4. An Interconnection Matrix

The signals generated by any master are Haddr, Hwdata, Htrans, Hwrite and Terminate. It receives the signals Hrdata and Hready from the slaves. The signals received by any master are Haddr, Hwdata, Htrans, Hwrite and Terminate. It generates the signals Hrdata and Hready to be sent to corresponding masters with which it performs data transfer. The Interconnect Matrix is present for the proper routing of address and data between masters and slaves. It also performs the arbitration process to determine which master should be allowed to perform data transfer.

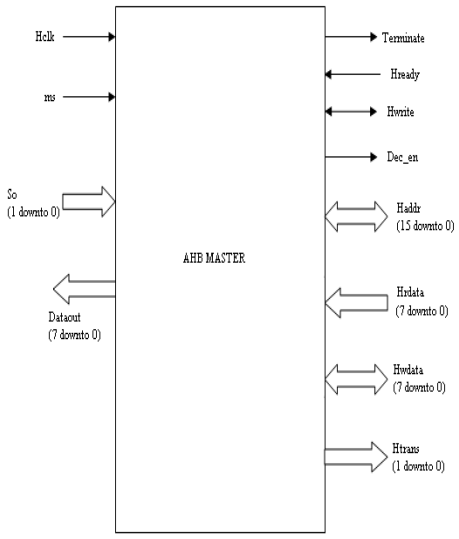

Fig 4: Multi-layer AHB master

All the operations of the master must begin at the rising edge of HCLK. Each master has an input pin called MS (master select). Only when this pin is high will the master be enabled and ready for operation.

Whenever the master select signal is high immediately in the next clock cycle the master should generate a 16 bit address. The master should also generate appropriate control signal such as HWRITE and HTRANS to determine whether the master intends to perform write operation or read operation.

The generation of these signals is based on the select operation signal and the HADDR signals. All the AMBA AHB signals must be generated only by the master and should not be modified externally by the driver. One of the most important properties of an AHB master is that it must be capable of performing pipelining operation. This means in the first clock cycle after the master select is high the master must generate only the 16 bit address.

In the next clock cycle the master must generate the 8 bit data to be written in the address. In the same clock the master must also generate the next address. This is done to reduce the time of data transfer and hence achieve high performance [5].

Pipelining is achieved by using an internal signal called addr_gen which determines at which clock cycles the address must be generated. All the masters must be capable of generating address and data. This is achieved by implementing an internal ROM architecture. A counter is implemented and depending upon its value at each clock cycle a new address and data will be generated. The address and data generation must be dependent on the HREADY signal generated by the corresponding slave which determines whether or not the slave is ready to sample the address and data sent by the master. Hence whenever the signal HREADY is low the master

introduces a wait state. The other control signal generated by master is HTRANS. It is used to determine the state of operation of the master.

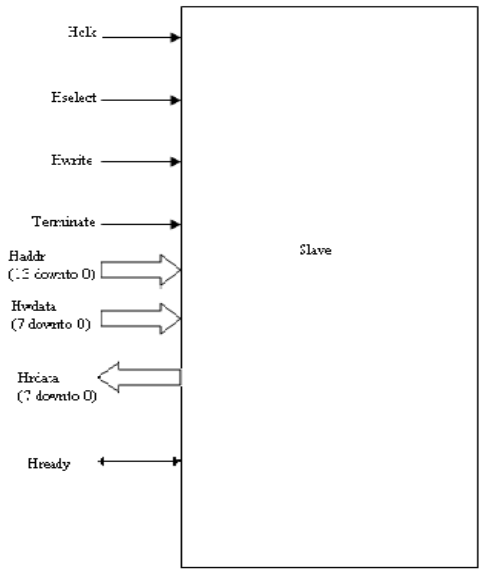

Fig 5: Multi-layer AHB slave

The slave is basically a memory element. Each of the slaves designed consists of 16 kilo bytes of memory. The slaves by itself cannot initiate any operation. It can just respond to the signals generated by the master and hence it is called a "slave". The slave will capture the address and data sent by the master. The slave then converts this address into an integer. It then uses this integer value as an index to the appropriate location of the memory. It is from this memory location that the slave will either write the data sent by the master or read from this memory location depending on whether the master intends to perform write or read operation.The slave performs write or read operation depending on the HWRITE signal generated by the master. Whenever this HWRITE signal is high, it means that the master intends to perform write operation and hence the data generated in the next clock cycle will be sampled and stored in the memory.

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5 SIMULATION RESULT

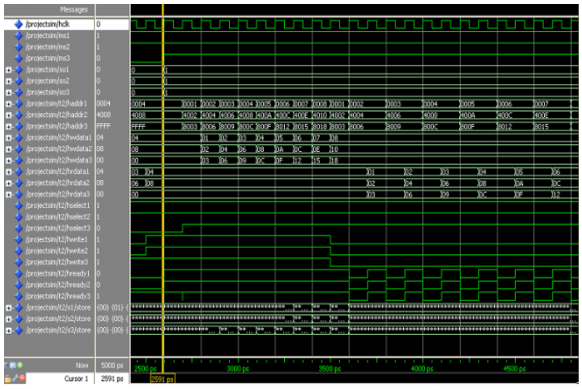


Fig 7: Burst of read followed by burst of write

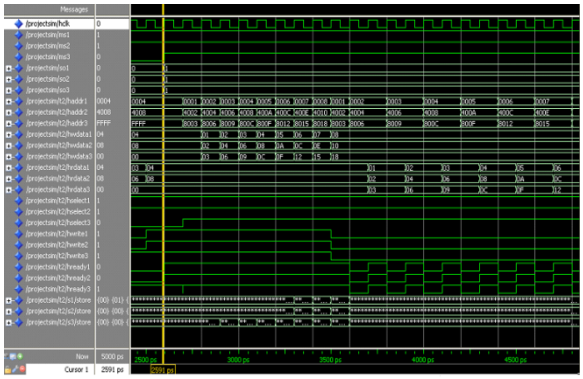
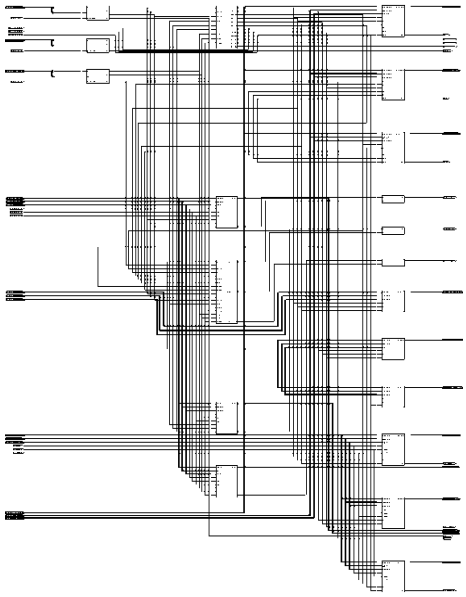


Fig8: Three Masters communicating with three slaves

6 RTL SCEMATIC OF INTER CONNECT MATRIX



7 CONCLUSION

In situations where the system bottleneck is the result of limited bandwidth across the system bus, multi-layer AHB solves the issue by multiplying the available bandwidth in proportion to the number of bus layers. Additional benefits arise from the reduction in bus transaction latency as a result of increased bus capacity.

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